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REMARKS

The Applicants request reconsideration of the rejection.

Claims 31-37 are now pending.

In light of the cancellation of Claims 1-30, the rejections under 35 U.S.C. 112, 102, and 103 are avoided, without admission as to the propriety.

New Claims 31-37 are clear of the prior art, and avoid the possible informalities noted by the Examiner. In particular, the new claims are patentably distinguishable from the primary reference to Shirakawa et al., U.S. 5,831,833 (Shirakawa), which discloses a method of manufacturing bare chip mounting multi-layer printed circuit boards, but which does not disclose or fairly suggest a power amplifier module having upper and lower semiconductor chips as claimed in the new claims. Although Shirakawa appears to disclose semiconductor chips 1 and 20 corresponding to the now-claimed first and second semiconductor chips, new Claim 31 requires a power amplifying circuit that is comprised of a multi-stage cascade connection of transistors, wherein the first semiconductor chip includes a final-stage transistor in the multi-stage cascade connection, and wherein the second

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semiconductor chip includes a control-use transistor which controls the final-stage transistor. Further, the power amplifier module of Claim 31 requires a module board over which the first and second semiconductor chips are overlappingly disposed, wherein the module board has an electrically conductive support on an upper surface thereof, which supports the second semiconductor chip and which is electrically connected with a reference potential electrode formed on a lower surface of the second semiconductor chip. Shirakawa neither discloses nor suggests these features, whether taken individually or in combination with any other reference of record.

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In view of the new claims and the foregoing remarks, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,

  
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